

Preliminary Amendment

Applicant: Javier Argüelles

Serial No.: 10/717,214

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Docket No.: I435.105.101

Title: PROCESS AND DEVICE FOR TESTING A SERIALIZER CIRCUIT ARRANGEMENT AND PROCESS AND DEVICE FOR TESTING A DESERIALIZER CIRCUIT ARRANGEMENT

IN THE ABSTRACT

Please amend the Abstract as follows:

**PROCESS AND DEVICE FOR TESTING A SERIALIZER CIRCUIT ARRANGEMENT
AND PROCESS AND DEVICE FOR TESTING A DESERIALIZER CIRCUIT
ARRANGEMENT**

ABSTRACT~~Abstract~~

A process and a device are proposed for testing a serializer and deserializer circuit arrangement ~~(2, 3)~~, where to control the test sequence a simple digital interface ~~(+2)~~ is used. To test the serializer circuit arrangement ~~(2)~~ firstly the quality of a multiphase clock signal ~~(CLK)~~ of the serializer circuit arrangement ~~(2)~~ and secondly the ability to transmit a preset bit pattern are tested. To test the deserializer circuit arrangement ~~(3)~~ the quality of the multiphase clock signal ~~(CLK)~~ and the quality of a data eye obtained during clock and data recovery are tested together with the quality of the clock recovery.